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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,628	03/31/2004	Simon Knowles	ICER-321538	3813
27964	7590	12/17/2009	EXAMINER	
HITT GAINES P.C. P.O. BOX 832570 RICHARDSON, TX 75083			FRANKLIN, RICHARD B	
			ART UNIT	PAPER NUMBER
			2181	
			NOTIFICATION DATE	DELIVERY MODE
			12/17/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)
	10/813,628	KNOWLES, SIMON
	Examiner	Art Unit
	RICHARD FRANKLIN	2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 16 September 2009.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-29 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-29 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____ .	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

1. Claims 1 – 29 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 16 September 2009 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1 – 29 are have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2 – 5, 7 – 10, 17 – 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claims 2 – 5, 19 – 21, and 23 each recite the limitation "an instruction packet" in the body of each claim. There is insufficient antecedent basis for these limitations in the claims. It is not clear if the limitations are referring to the instruction packet recited in claim 1 or a new instruction packet.

The Examiner has interpreted the limitation as referring to the instruction packet of claim 1.

6. Claim 2 recites the limitation "the control process" in lines 2 and 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

7. Claims 7, 17, and 18 each recite the limitation "the data processing channel" in the body of each claim. There is insufficient antecedent basis for these limitations in the claims.

8. Claims 8 and 21 each recite the limitation "a memory access instruction" in the body of each claim. There is insufficient antecedent basis for these limitations in the claims. It is not clear if the limitations are referring to the memory access instruction recited in claim 1 or a new memory access instruction.

9. Claim 8 recites the limitation "a control instruction" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the control instruction recited in claim 1 or a new control instruction.

10. Claims 8, 23, and 25 each recite the limitation "a data processing instruction" in the body of each claim. There is insufficient antecedent basis for these limitations in the claims. It is not clear if the limitations are referring to the data processing instruction recited in claim 1 or new data processing instructions.

11. Claim 9 is also rejected because of its inheritance of the deficiencies of parent claim 8.

12. Claim 10 states that the second processing channel is dedicated to the performance of data processing operations. However, parent claim 1 states that the second processing channel performs both data processing operations and memory access operations. Therefore, it is not clear whether the second processing channel performs memory access operations and data processing operations, or ONLY performs data processing operations.

13. Claim 18 recites the limitation "the control processing channel" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

14. Claims 19 and 22 each recite the limitation "the bit length" in the body of each claim. There is insufficient antecedent basis for these limitations in the claims.

15. Claim 21 recites the limitation "a data processing operation" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the data processing instruction recited in claim 1 or a new data processing operation.

16. Claims 23 and 24 each recite the limitation "a control processing instruction" in the body of each claim. There is insufficient antecedent basis for these limitations in the claims. It is not clear if the limitations are referring to the control instruction recited in claim 1 or new control processing instructions.

17. Claim 26 recites the limitation "the decode unit" in line 15 of the claim. There is insufficient antecedent basis for this limitation in the claim.

18. Claims 27 and 28 are also rejected because of their inheritance of the deficiencies of parent claim 26.

19. Claim 29 recites the limitation "a control format" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the control format recited earlier in the claim or a new control format.

The Examiner has interpreted the limitation as referring to the control format recited earlier in the claim.

20. Claim 29 recites the limitation "a data processing instruction" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the data processing instruction recited earlier in the claim or a new data processing instruction.

The Examiner has interpreted the limitation as referring to the data processing instruction recited earlier in the claim.

21. Claim 29 recites the limitation "a data format" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim. It is not clear if the limitation is referring to the data format recited earlier in the claim or a new data format.

The Examiner has interpreted the limitation as referring to the data format recited earlier in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

22. Claim 29 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,292,845 (hereinafter Fleck).

As per claim 29, Fleck teaches a computer readable medium bearing an instruction set for a computer including a first class of instruction packets each

comprising two or more control instructions having a control format for execution sequentially (Fleck; Col 3 Lines 47 – 52) and a second class of instruction packets each comprising at least a data processing instruction having a data format and a further instruction for execution contemporaneously (Fleck; Col 3 Lines 34 – 47), said further instruction being selected from one or more of: a memory access instruction having a memory access format (Fleck; Col 3 Lines 25 – 52 "load/store instruction"); a control instruction having a control format (Fleck; Col 3 Lines 25 – 52 "branch or other special instructions"); and a data processing instruction having a data format (Fleck; Col 3 Lines 25 – 52 "data manipulation instructions" and "integer operation").

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

23. Claims 1 – 3, 6 – 10, 12, 14, 17, 19, and 21 – 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,292,845 (hereinafter Fleck) in view of US Patent Application Publication No. 2004/0054876 (hereinafter Grisenthwaite).

As per claim 1, Fleck teaches a computer processor (Fleck; Figure 1), the processor comprising: (a) a decode unit (Fleck; Figure 1 Item 7) for decoding a stream of instruction packets from a memory (Fleck; Figure 1 Item 3), each instruction packet comprising a plurality of instructions (Fleck; Col 3 Lines 15 – 17), each of the plurality of

instructions being one of the group comprising: a memory access instruction having a memory access format (Fleck; Col 3 Lines 25 – 52 "load/store instruction"); a control instruction having a control format (Fleck; Col 3 Lines 25 – 52 "branch or other special instructions"); and a data processing instruction having a data format (Fleck; Col 3 Lines 25 – 52 "data manipulation instructions" and "integer operation"); (b) a first processing channel comprising a plurality of functional units (Fleck; Figure 1 Items 8 and 10) and operable to perform control processing operations and memory access operations (Fleck; Col 3 Lines 28 – 30); (c) a second processing channel comprising a plurality of functional units (Fleck; Figure 1 Items 9 and 11) and operable to perform data processing operations (Fleck; Col 3 Lines 30 – 32); wherein the decode unit is operable to receive an instruction packet and to detect if the instruction packet defines (i) at least two control instructions (Fleck; Col 3 Lines 47 – 52) or (ii) a plurality of instructions one or more of which is a data processing instruction (Fleck; Col 3 Lines 34 – 47), and wherein when the decode unit detects that the instruction packet comprises at least two control instructions said control instructions are supplied to the first processing channel for execution in program order (Fleck; Col 3 Lines 47 – 52).

Fleck does not explicitly teach wherein the second processing channel also performs memory access operations.

However, Grisenthwaite teaches that in a processor with two pipelines, the first and second pipelines can execute the same types of instructions (Grisenthwaite; Paragraph [0029] Lines 1 – 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck to include the memory access operations in the second processing channel because doing so allows for improved throughput of instructions through the processor (Grisenthwaite; Paragraph [0029] Lines 1 – 9).

As per claim 2, Fleck also teaches the decode unit is operable to detect an instruction packet comprising three control instructions and control the control process to execute each of the three control instructions in the order in which they appear in the instruction packet (Fleck; Col 3 Lines 34 – 52; Examiner's note: Since the instruction buffer contains four instructions and the instructions may be of the same type, it is clear that Fleck discloses the ability to decode three control instructions).

As per claim 3, Fleck also teaches wherein the decode unit is operable to detect an instruction packet containing a plurality of control instructions of equal length (Fleck; Col 3 Lines 34 – 52).

As per claim 6, Fleck also teaches wherein the decode unit is operable to receive and decode instruction packets of a bit length of 64 bits (Fleck; Col 3 Lines 9 – 12).

As per claim 7, Grisenthwaite also teaches wherein the decode unit is operable to detect when there is at least one data processing instruction and in response thereto,

to cause relevant data to be supplied to the data processing channel (Grisenthwaite; Paragraph [0043] Lines 4 – 8).

As per claim 8, Fleck also teaches wherein the decode unit is operable to detect that the instruction packet comprises at least one data processing instruction (Fleck; Col 4 Lines 11 – 16) and a further instruction selected from one or more of: a memory access instruction (Fleck; Col 4 Lines 11 – 16); a control instruction; and a data processing instruction.

As per claim 9, Fleck also teaches wherein at least one data processing instruction and said further instruction are executed in parallel (Fleck; Col 3 Lines 25 – 28).

As per claims 10 and 25, Fleck teaches the second processing channel performs data processing operations (Fleck; Col 3 Lines 30 – 32) and data processing instructions are provided in assembly language (Fleck; Col 4 Lines 63 – 67; Examiner's Note: It would have been common at the time of invention to require the instructions to be written in assembly code as was a common standard at the time of invention.).

As per claim 12, Fleck also teaches wherein the first processing channel comprises a load/store unit (Fleck; Figure 1 Item 10).

As per claim 14, Fleck also teaches wherein the second processing channel comprises a data execution path including a fixed data execution unit (Fleck; Figure 1 Item 11).

As per claim 17, Fleck also teaches wherein the data processing channel comprises a load/store unit (Fleck; Figure 1 Item 10).

As per claim 19, Fleck also teaches wherein the decode unit is operable to detect an instruction packet comprising at least one data processing instruction, wherein the bit length of the at least one data processing instruction is between 30 and 38 bits (Fleck; Figure 2 Items 213, 214, and 217).

As per claim 21, Fleck also teaches wherein the decode unit is operable to detect that the instruction packet comprises a data processing instruction (Fleck; Col 4 Lines 11 – 16) and a memory access instruction (Fleck; Col 4 Lines 11 – 16).

As per claim 22, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 21 (see rejection of claim 21 above).

Fleck in combination with Grisenthwaite does not explicitly disclose the bit length of said memory access instruction is 28 bits.

However, it would have been obvious to one of ordinary skill in the art at the time of invention that the bit lengths of instructions disclosed in Fleck and Grisenthwaite are

of little significance and the primary concern set forth by Fleck and Grisenthwaite is merely the separation of instructions within the packet. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a smaller instruction size than 32 bits in the invention disclosed by Fleck with the goals of either saving space or adapting the invention to a customized standard. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of invention that the size of an individual word is of no consequence given the words are still separated properly as disclosed by Fleck.

As per claim 23, Fleck also teaches wherein the decode unit is operable to detect that the instruction packet comprises a data processing instruction (Fleck; Col 4 Lines 11 – 16) and a control processing instruction (Fleck; Col 3 Lines 28 – 30, Col 4 Lines 11 – 16).

As per claim 24, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Fleck in combination with Grisenthwaite does not explicitly disclose the decode unit being operable to detect a control processing instruction in C code or variant thereof.

However, it would have been obvious to one of ordinary skill in the art at the time of invention to enable a processor to support higher level languages, such as C, as the languages are easier to develop code in and are more commonly used to develop code

in. Therefore, it would have been obvious to allow a user to utilize an easier language such as C to code control instructions.

As per claims 26 – 28, Fleck teaches a method of operating a computer processor which comprises a first and second processing channels (Fleck; Figure 1 Items 8 – 11), each having a plurality of functional units, wherein the first processing channel is capable of performing control processing operations and memory access operations (Fleck; Col 3 Lines 28 – 30), and the second processing channel is capable of performing data processing operations (Fleck; Col 3 Lines 30 – 32), the method comprising: (a) receiving a sequence of instruction packets from a memory (Fleck; Figure 1 Item 3), each of said instruction packets comprising a plurality of instructions defining operations (Fleck; Col 3 Lines 15 – 17), each of the plurality of instructions being one of the group comprising: a memory access instruction having a memory access format (Fleck; Col 3 Lines 25 – 52 "load/store instruction"); a control instruction having a control format (Fleck; Col 3 Lines 25 – 52 "branch or other special instructions"); and a data processing instruction having a data format (Fleck; Col 3 Lines 25 – 52 "data manipulation instructions" and "integer operation"); (b) decoding each instruction packet in turn by determining if the instruction packet defines: (i) at least two control instructions (Fleck; Col 3 Lines 47 – 52); or (ii) at least one data processing instruction (Fleck; Col 3 Lines 34 – 47), and wherein when the decode unit detects that the instruction packet comprises at least two control instructions supplying said at least

two control instructions to said first processing channel for execution in sequence (Fleck; Col 3 Lines 47 – 52).

Fleck does not explicitly teach wherein the second processing channel also performs memory access operations.

However, Grisenthwaite teaches that in a processor with two pipelines, the first and second pipelines can execute the same types of instructions (Grisenthwaite; Paragraph [0029] Lines 1 – 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck to include the memory access operations in the second processing channel because doing so allows for improved throughput of instructions through the processor (Grisenthwaite; Paragraph [0029] Lines 1 – 9).

24. Claims 4 – 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,292,845 (hereinafter Fleck) in view of US Patent Application Publication No. 2004/0054876 (hereinafter Grisenthwaite) and further in view of US Patent No. 6,880,150 (hereinafter Takayama).

As per claim 4, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 3 (see rejection of claim 3 above).

Fleck in combination with Grisenthwaite does not teach detecting within an instruction packet a control instruction of a bit length between 18 and 24 bits.

However, Takayama teaches detecting within an instruction packet a control instruction of a bit length between 18 and 24 bits (Takayama; Col 13 Lines 29 – 33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck in combination with Grisenthwaite to include the control packet of between 18 and 24 bits in length because doing so allows for control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col 2 Lines 9 – 13) which increases execution speed of control instructions and thus the entire system.

As per claim 5, Takayama also teaches detecting within an instruction packet a plurality of control instructions each having a bit length of 21 bits (Takayama; Col 13 Lines 29 – 33).

As per claim 11, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Fleck in combination with Grisenthwaite does not teach control processing operations being performed on operands up to a first predetermined bit width and the data processing operations being performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width.

However, Takayama teaches control processing operations being performed on operands, up to a first predetermined bit width and the data processing operations being performed on data up to a second pre-determined bit width, the second pre-determined bit width being larger than the first pre-determined bit width (Takayama; Col 13 Lines 29 – 33; Examiner's note: Use of 21-bit and 42-bit instructions.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck in combination with Grisenthwaite to include the pre-determined bit widths because doing so allows for control instructions to be executed even when other operations are performed in units of an integer number of bytes (Takayama; Col 2 Lines 9 – 13).

25. Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,292,845 (hereinafter Fleck) in view of US Patent Application Publication No. 2004/0054876 (hereinafter Grisenthwaite) and further in view of US Patent No. 5,956,518 (hereinafter DeHon).

As per claim 13, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Fleck in combination with Grisenthwaite does not teach the second processing channel comprising a data execution path including a configurable data execution unit.

However, DeHon teaches a data execution path including a configurable data execution unit (DeHon; Col 5 Lines 23 – 26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck in combination with Grisenthwaite to include the configurable data execution unit because doing so allows for greater flexibility for processing ability (DeHon; Col 1 Lines 41 – 47).

As per claim 15, DeHon also teaches wherein the configurable data execution unit operates according to single instruction multiple data principles (DeHon; Col 5 Lines 23 – 26).

26. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,292,845 (hereinafter Fleck) in view of US Patent Application Publication No. 2004/0054876 (hereinafter Grisenthwaite) and further in view of US Patent No. 7,234,042 (hereinafter Wilson).

As per claim 16, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 14 (see rejection of claim 14 above).

Fleck in combination with Grisenthwaite does not teach wherein the fixed data execution unit operates according to single instruction multiple data (SIMD) principles.

However, Wilson teaches a fixed data execution unit which performs per SIMD principles (Wilson; Col 3 Line 52 – Col 4 Line 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck in combination

with Grisenthwaite to include the SIMD because doing so allows for an improved flexibility of an instruction set (Wilson; Col 1 Lines 36 – 38).

27. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,292,845 (hereinafter Fleck) in view of US Patent Application Publication No. 2004/0054876 (hereinafter Grisenthwaite) and further in view of US Patent No. 6,725,357 (hereinafter Cousin).

As per claim 18, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 1 (see rejection of claim 1 above).

Fleck in combination with Grisenthwaite does not teach wherein a single load/store unit is accessed by both channels through respective ports.

However, Cousin teaches two processing channels which access a single common load/store unit through respective ports (Cousin; Figure 3 Item 150).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck in combination with Grisenthwaite to include the single load/store unit because doing so allows for the channels to work together to accomplish instructions (Cousin; Col 5 Line 56 – Col 6 Line 4).

28. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,292,845 (hereinafter Fleck) in view of US Patent Application Publication No. 2004/0054876 (hereinafter Grisenthwaite) and further in view of "Variable Length

Instruction Compression for Area Minimization", Piia Simonen, Ilkka Saastamoinen, Jari Nurmi, 2003, IEEE (hereinafter Simonen).

As per claim 20, Fleck in combination with Grisenthwaite teaches the computer processor as described per claim 19 (see rejection of claim 19 above). Fleck in combination with Grisenthwaite further disclose the decode unit being operable to detect an instruction packet comprising at least one data processing instruction.

Fleck in combination with Grisenthwaite does not teach a bit length of the at least one data processing instruction is 34 bits.

However, Simonen teaches a bit length of the at least one data processing instruction is 34 bits (Simonen; Section 3.1 ("Control Bits") Lines 3 – 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Fleck in combination with Grisenthwaite to include the 34 bit data processing instruction because doing so allows for a reduction in the amount of space needed to implement certain data processing instructions (Simonen; Section 1 Lines 1 – 4, Section 3.1 Lines 5 – 7) which would increase overall processor throughput.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD FRANKLIN whose telephone number is (571)272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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